

Amendments to the Claims:

The listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claims 1 – 2 (cancelled)

Claim 3. (currently amended) A programmable controller for use with a monitoring device, said programmable controller including:

at least one digital input interface ~~and an input register for connection to process plant and/or machinery to provide sampled and stored input data in digital form,~~

at least one digital output interface for receiving data from at least one output register ~~connection to process plant and/or machinery to receive output data in digital form,~~

programmable logic hardware including a plurality of basic logic elements and electrically configurable interconnections, said interconnections configurable to interconnect the logic elements as a logic circuit, said logic circuit arranged to implement a user control program defined by a user as a user program circuit, said logic circuit configurable in said programmable logic hardware, and connected to said input interfaces and said ~~and to connect the user control program circuit to said input and output interfaces,~~

program loading circuits ~~means~~ to enable the user to configure the programmable logic hardware with as a circuit including said user program circuit implementing a user control program prior to initiating control, and wherein: ~~of the associated process plant and/or machinery,~~

~~— a user control program implemented as an electrical logic circuit configured in said programmable logic hardware is configured including at least two functionally separate subsystems, a first subsystem comprising said user program circuit, and a second subsystem to provide monitoring services and to control the operation of , with said user program circuit, connected to said input and output interfaces and wherein:~~

~~said first subsystem said programmable logic as configured~~ has a plurality of flip-flops combined with gating circuits, wherein one of said flip-flops combined with one of said gating circuits forms a dual purpose flip-flop for storing state data in said state data storage units storing the user program circuit, said dual purpose flip-flops, when connected in said user program circuit, are selectively operable in a first way as a shift chain operable to provide both read and write access to said state data or in a second way as logic elements of said user program circuit, only one of said first way or said second way being operative at any one time-state data, and a means of access to said state data storage units,

~~—— a monitoring device may be connected via said means of access to said state data storage units, and~~

~~—— said means of access to said state data storage units enables said monitoring device to read data values from said state data storage units and to write data values to said state data storage units while the user control program continues to perform control functions.~~

Claim 4. (currently amended) The programmable controller as claimed in claim 3, ~~with an operating cycle of at least two non-overlapping sequential intervals, and wherein,~~

said second subsystem enables the control and operation of said user program circuit in a plurality of modes of operation in response to commands from the monitoring computer, said modes of operation including:

—— a logic processing mode in which said dual purpose flip-flops are operated as said logic elements in said user program circuit, and in which the clock to said dual purpose flip-flops is enabled, or

—— a pause mode in which the clock to said dual purpose flip-flops is disabled, and wherein either said logic processing mode or said pause mode may be temporarily interrupted by a data access mode in which said dual purpose flip-flops are operated as part of a shift chain so that enabling the clock to said dual purpose flip-flops shifts the state data in said dual purpose flip-flops and provides both read and write access~~said input register operates to sample and store the input data within a first said interval ("logic processing interval");~~

~~—— said programmable logic circuit includes clocking means that applies clock pulses in said logic processing interval as required by the user control program circuit, said logic processing interval allowing the user control program circuit signals to settle, and~~

~~_____ said means of access to said data storage units enable said monitoring device to read data from and/or write to said state data storage units during a second said interval ("data access interval").~~

Claims 5 – 7 (cancelled)

Claim 8. (previously presented) The programmable controller as claimed in claim 4 with duplicated hardware to facilitate program swapping operations including:

at least two separately configurable sections of programmable logic hardware for separately configurable user control program circuits,

output selector means to selectively connect one of said programmable logic hardware sections to said output interfaces via the output register, and

state data relocation means for writing, within one data access interval, state data from an outgoing said programmable logic hardware section to the state data storage units of an incoming said programmable logic hardware section that have the same user control program functions as those from which it was read.

Claim 9. (previously presented) The programmable controller as claimed in claim 8, wherein said state data relocation means comprises:

relocation address storage writable by said monitoring device, corresponding with said state data storage units,

secondary state data storage to save data from said state data storage units,

selection means for selecting either a non-relocated address or a relocated address with which to access said secondary state data storage, and

data relocation means for performing, within one said data access interval, the steps of:

- (i) reading a state data bit from said outgoing programmable logic hardware section,
- (ii) writing said state data bit into said secondary state data storage at an address stored in said relocation address storage,
- (iii) repeating steps (i) and (ii) until all required bits have been relocated and transferred,

- (iv) reading a state data bit from said secondary state data storage,
- (v) writing said state data bit into said incoming programmable logic hardware section at the same address at which it was located in said secondary state data storage, and
- (vi) repeating steps (iv) and (v) until all required bits have been transferred.

Claim 10. (previously presented) A programmable controller said programmable controller including:

at least one input interface and an input register for connection to process plant and/or machinery to provide sampled and stored input data in digital form,

at least one output interface for connection to process plant and/or machinery to receive output data in digital form,

programmable logic hardware including a plurality of basic logic elements and electrically configurable interconnections, said interconnections configurable to interconnect the logic elements as a user control program circuit and to connect the user control program circuit to said input and output interfaces,

program loading means to enable the user to configure the programmable logic hardware as a circuit implementing a user control program prior to initiating control of the associated process plant and/or machinery,

a user control program implemented as an electrical logic circuit configured in said programmable logic hardware, with said user program circuit connected to said input and output interfaces and means to support circuit failure detection including

at least two separately configurable sections of programmable logic hardware configurable with identical user control program circuits, said input register providing identical settled input values, that are not transient at the time of sampling by the user control program circuit, to each user control program circuit, and,

failure detection means comparing a set of output values of each said programmable logic section with the corresponding set of output values of each other section, and indicating failure of said programmable logic hardware if the sets of settled output values of said sections are not identical.

Claim 11. (previously presented) A programmable controller said programmable controller including:

at least one input interface and an input register for connection to process plant and/or machinery to provide sampled and stored input data in digital form,

at least one output interface for connection to process plant and/or machinery to receive output data in digital form,

programmable logic hardware including a plurality of basic logic elements and electrically configurable interconnections, said interconnections configurable to interconnect the logic elements as a user control program circuit and to connect the user control program circuit to said input and output interfaces,

program loading means to enable the user to configure the programmable logic hardware as a circuit implementing a user control program prior to initiating control of the associated process plant and/or machinery,

a user control program implemented as an electrical logic circuit configured in said programmable logic hardware, with said user program circuit connected to said input and output interfaces and

means to support circuit failure detection and connection including:

at least three said separately configurable sections of programmable logic hardware configurable with identical user control program circuits, said input register providing identical settled input values, that are not transient at the time of sampling by the user control program circuit, to each user control program circuit, and

failure detection means to compare a set of output values of each said programmable logic hardware section with the corresponding set of output values of at least two other said sections, and

output processing means to pass a set of correct output values to the control outputs via the output register and ensure incorrect output values as indicated by said failure detection means do not propagate to the control outputs;

wherein said failure detection means determines that a programmable logic hardware section has failed if the set of settled output values of said programmable logic hardware section is not identical to at least one of the sets of settled output values of the other programmable logic hardware sections, identifies any unmatched sets of outputs as coming from a failed programmable logic hardware section, and indicates the failure of that

programmable logic hardware section.

Claim 12. (previously presented) The programmable controller as claimed in claim 10 including a plurality of said failure detection means with the sets of outputs from each section of programmable logic hardware provided as inputs to each said failure detection means, and

detection of a failure by any one of the two or more failure detection means indicates that a failure has occurred.

Claim 13. (previously presented) The programmable controller as claimed in claim 11 including a plurality of said failure detection and correction means with the sets of outputs from each of the at least three sections of programmable logic hardware provided as inputs to each of the failure detection and correction means, and wherein:

indication of a difference between the sets of output values of any two sections of programmable logic hardware by any one or more of the failure detection means indicates that a failure has occurred, and

at least two or more failure detection circuits must agree that a particular section of programmable logic hardware is operating correctly before the set of output values from that said section is deemed to be correct, and

said output processing means passes a set of correct output values to the control outputs via the output register and ensures incorrect output values, as indicated by said failure detection means, are not propagated to the control outputs.

Claim 14. (previously presented) The programmable controller as claimed in claim 13 including exception evaluating and handling means which ensures that the controller responds appropriately when the number of sets of concurrently correct output values deemed desirable as a safety margin does not exist, the minimum said number being two.

Claim 15. (previously presented) The programmable controller as claimed in claim 3 wherein said programmable controller receives input signals from duplicate sensors and said user control program includes at least one input signal monitoring function block, said monitoring block determining the invalidity of an input signal by a comparison of said

duplicate input signals using criteria defined as part of the function block as suitable to identify signals in error, and indicating an input signal error if said input signal is deemed invalid.

Claim 16. (previously presented) The programmable controller as claimed in claim 15 wherein said duplicate sensors include three or more matching sensors and the respective said input signal monitoring function block determines the invalidity of an input signal from a comparison of said matching input signals, and determines the invalid signal as the odd-one-out, and passes a single copy of the valid signals as the input signal.

Claim 17. (previously presented) The programmable controller as claimed in claim 4 including means to support circuit failure detection including

at least two separately configurable sections of programmable logic hardware configurable with identical user control program circuits, said input register providing identical settled input values, that are not transient at the time of sampling by the user control program circuit, to each user control program circuit, and,

failure detection means comparing a set of output values of each said programmable logic section with the corresponding set of output values of each other section, and indicating failure of said programmable logic hardware if the sets of settled output values of said sections are not identical.

Claim 18. (previously presented) The programmable controller as claimed in claim 4 including means to support circuit failure detection and correction including:

at least three said separately configurable sections of programmable logic hardware configurable with identical user control program circuits and with identical input values, and

said identical input valves provided in a way so as to be settled and not transient at the time of sampling by the user control program circuit, and

failure detection means to compare a set of output values of each said programmable logic hardware section with the corresponding set of output values of at least two other said sections, and

output processing means to pass a set of correct output values to the control outputs

via the output register and ensure incorrect output values as indicated by said failure detection means do not propagate to the control outputs;

wherein said failure detection means determines that a programmable logic hardware section has failed if the set of settled output values of said programmable logic hardware section is not identical to at least one of the sets of settled output values of the other programmable logic hardware sections, identifies any unmatched sets of outputs as coming from a failed programmable logic hardware section, and indicates the failure of that programmable logic hardware section.

Claim 19. (previously presented) The programmable controller as claimed in claim 18 including a plurality of said failure detection and correction means with the sets of outputs from each of the at least three sections of programmable logic hardware provided as inputs to each of the failure detection and correction means, and wherein:

indication of a difference between the sets of output values of any two sections of programmable logic hardware by any one or more of the failure detection means indicates that a failure has occurred, and

at least two or more failure detection circuits must agree that a particular section of programmable logic hardware is operating correctly before the set of output values from that said section is deemed to be correct, and

said output processing means passes a set of correct output values to the control outputs via the output register and ensures incorrect output values, as indicated by said failure detection means, are not propagated to the control outputs.

Claims 20 – 21(cancelled)

Claim 22. (currently amended) The programmable controller as claimed in claim 4, ~~wherein-21 including:~~

said programmable controller may be set to operate said user program circuit in said logic processing mode, and when so set is able to respond to the monitoring computer to enable access to the state data in said user program circuit and in so doing said user program circuit enters said data access mode, and during such an instance of said data access mode entered from a said logic processing mode, said output registers

maintain the system output signals at the levels last established by said logic processing mode, but when data access is complete, said user program circuit is automatically switched back to said logic processing mode and said user program circuit again updates said output registers, and

said programmable controller may be set to operate said user program circuit in said pause mode, and when so set is able to respond to the monitoring computer to enable access to said user program circuit state data and in so doing said user program circuit enters said data access mode, but when data access is complete, said user program circuit is automatically switched back to said pause mode~~an output register to store said output data for said output interface, and wherein~~

~~—— said user control program circuit includes dual purpose flip-flops, each dual purpose flip-flop for providing the normal logic processing circuit storage function of storing said user program state data and transporting said user program state data into and out of the user control program circuit.~~

Claim 23. (previously presented) The programmable controller as claimed in claim 22 with duplicated hardware to facilitate program swapping operations including:

at least two separately configurable sections of programmable logic hardware for separately configurable user control program circuits,

output selector means to selectively connect one of said programmable logic hardware sections to said output interfaces via the output register, and

state data relocation means for writing, within one data access interval, state data from an outgoing said programmable logic hardware section to the state data storage units of an incoming programmable logic hardware section that have the same user control program functions as those from which it was read.

Claim 24. (previously presented) The programmable controller as claimed in claim 23, wherein said state data relocation means comprises:

relocation address storage writable by said monitoring device, corresponding with said state data storage units,

secondary state data storage to save data from said state data storage units,

selection means for selecting either a non-relocated address or a relocated address with which to access the said secondary state data storage, and

data relocation means for performing, within one said data access interval, the steps of:

- (i) reading a state data bit from a programmable logic hardware section,
- (ii) writing said state data bit into said secondary state data storage at an address stored in said relocation address storage,
- (iii) repeating steps (i) and (ii) until all required bits have been relocated and transferred,
- (iv) reading a state data bit from said secondary state data storage,
- (v) writing said state data bit into the same or a different programmable logic hardware section at the same address at which it was located in said secondary state data storage, and
- (vi) repeating steps (iv) and (v) until all required bits have been transferred.

Claim 25. (previously presented) The programmable controller as claimed in claim 22 including means to support state data modification comprising:

secondary modification data storage corresponding to said state data storage units, and

a modification indicator corresponding to each said state data storage unit, said modification indicator and the contents of said secondary storage being writable by said monitoring device; and

data modification means operative to perform within one said data access interval the steps of:

scanning said modification indicators,

loading data stored in said secondary modification data storage units to said corresponding state data storage units if the corresponding modification indicator so indicates, and

resetting said modification indicators.

Claim 26. (previously presented) The programmable controller as claimed in claim 22 including means to support state data forcing comprising:

secondary modification data storage corresponding with said state data storage units;
a data forcing indicator for each said storage unit, said data forcing indicator and the contents of said secondary storage being writable by said monitoring device; and

data modification means for performing within one said data access interval the steps of:

scanning said data forcing indicators,

loading data stored in said secondary storage units to said corresponding state data storage units if the corresponding data forcing indicator so indicates,

without resetting said data forcing indicators.

Claim 27. (currently amended) The programmable controller as claimed in claim 22 arranged to enable program swapping with said programmable logic hardware being arranged in sections separately configurable including:

an outgoing section, with which items qualified by the term "outgoing" are associated, and including an outgoing user program circuit operating in said logic processing mode, and

an incoming section, with which items qualified by the term "incoming" are associated, being currently inoperative, and

performing in order the steps of:

configuring into said incoming section an incoming logic circuit including an incoming user program circuit, said incoming user program circuit being a modification of said outgoing user program circuit,

switching the mode of said outgoing user program circuit to pause mode and preserving the value stored in said output registers,

reading the state data from said outgoing user program circuit,

writing the state data from said outgoing user program circuit into the corresponding incoming state data storage units so that each state data bit in said incoming user program circuit that has a functional equivalent in said outgoing user program circuit has its state set to the same state that existed in the functionally equivalent bit in said outgoing user program circuit, and in the process relocating state data bits into different physical locations in said incoming section as compared to the physical locations in said outgoing section from which they were read, and

switching the mode of said incoming user program circuit to said logic processing mode and enabling said output registers to be updated,
wherein a functionally equivalent bit is a bit in one of the user program circuits, either said incoming user program circuit, or said outgoing user program circuit, that has identical meaning and function as that of a bit in the other user program circuit, to which it is therefore functionally equivalent, such functionally equivalent bits always existing in pairs
~~including means to support program swap operations, for performing, during said data access interval, the steps of:~~

~~—— reading and storing state data from said state data storage units,~~
~~—— configuring a new user control program in said programmable logic by reconfiguring said programmable connections; and~~
~~—— writing said stored state data, or modified stored state data, to corresponding newly configured state data storage units.~~

Claim 28. (currently amended) The programmable controller as claimed in claim 27 including circuits to support relocation of user program circuit state data from said outgoing section into functionally equivalent user program circuit state data storage units in said incoming section including:

cross-referencing circuits arranged to provide the address of a first functionally equivalent bit in a pair as a function of the address of the second functionally equivalent bit in the same pair of functionally equivalent bits~~including means to support relocation of state data from the outgoing programmable logic hardware section to the corresponding state data storage unit in the incoming programmable logic hardware section including:~~

~~relocation address storage corresponding with said state data storage units,~~
~~secondary state data storage to save data from said state data storage units,~~
~~selection means to select either a non-relocated address or a relocated address with which to access the said secondary state data storage, and~~

~~data relocation means performing the steps of:~~

- ~~(i) —— loading said relocation address storage with addresses supplied by said monitoring device; and within one said data access interval,~~
- ~~(ii) —— reading a state data bit from a programmable logic hardware section,~~

- ~~(iii) — writing said state data bit into said secondary state data storage at an address stored in said relocation address storage,~~
- ~~(iv) — repeating steps (ii) and (iii) until all required bits have been relocated and transferred,~~
- ~~(v) — reading a state data bit from said secondary state data storage,~~
- ~~(vi) — writing said state data bit into the same or a different programmable logic hardware section at the same address at which it was located in said secondary state data storage, and~~
- ~~(vii) — repeating steps (v) and (vi) until all required bits have been transferred.~~

Claim 29. (previously presented) The programmable controller as claimed in claim 4 with duplicated hardware to facilitate program swapping operations including:

at least two separately configurable sections of programmable logic hardware for separately configurable user control program circuits,

output selector means to selectively connect one of said programmable logic hardware sections to said output interfaces via the output register,

an outgoing user control program in a said section of the programmable logic hardware and,

a new user control program in another said programmable logic hardware section not connected to said output interface.

Claim 30. (previously presented) The programmable controller as claimed in claim 29 including:

state data from the outgoing said programmable logic hardware section written to the state data storage units of said programmable hardware section holding said new user control program that have the same user control program functions as those from which it was read.

Claim 31. (new) The programmable controller as claimed in claim 22 arranged to enable program swapping within a single section of programmable logic hardware, including:

an outgoing logic circuit, with which items qualified by the term “outgoing” are associated, and including an outgoing user program circuit operating in said logic processing mode, and

an incoming logic circuit, with which items qualified by the term “incoming” are associated, being currently inoperative, and

performing in order the steps of:

switching the mode of said outgoing user program circuit to pause mode and preserving the value stored in said output registers,

reading the state data from said outgoing user program circuit,

configuring into said single section of programmable logic hardware an incoming logic circuit including an incoming user program circuit, said incoming user program circuit being a modification of said outgoing user program circuit,

writing the state data from said outgoing user program circuit into the corresponding incoming state data storage units so that each state data bit in said incoming user program circuit that has a functional equivalent in said outgoing user program circuit has its state set to the same state that existed in the functionally equivalent bit in said outgoing user program circuit, and in the process relocating state data bits into different physical locations in said single section of programmable logic hardware as compared to the physical locations in said single section of programmable logic hardware from which they were read, and

switching the mode of said incoming user program circuit to said logic processing mode and enabling said output registers to be updated, wherein a functionally equivalent bit is a bit in one of the user program circuits, either said incoming user program circuit, or said outgoing user program circuit, that has identical meaning and function as that of a bit in the other user program circuit, to which it is therefore functionally equivalent, such functionally equivalent bits always existing in pairs.

Claim 32. (new) The programmable controller as claimed in claim 27 further arranged to allow the continuance of circuit operation after the occurrence of a circuit

operational failure of a type that does not cause permanent physical damage to said programmable controller, including:

at least three separately configurable blocks of programmable logic hardware, each said block being equivalent to one said outgoing section and one said incoming section, and performing in order the steps of:

operating each said block in parallel and in synchronism,

identifying circuit failures, by comparing on a clock-by-clock basis the operation of each said block against each other said block, and determining when at least one said block operates differently to the other said blocks,

reconfiguring each said block that has failed and placing the non-failing said blocks in said pause mode thus preserving the value stored in said output registers,

transferring the state of the non-failing said blocks to the reconfigured said block(s), and

restarting said blocks in said logic processing mode in parallel and in synchronism and enabling said output registers to be updated.